11-30-00

A

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.ATI010002 Total Pages 24
First Inventor or Application Identifier Rosefield, et al.
Title **APPARTUS HAVING REDUCED INPUT OUTPUT AREA AND METHOD THEREOF**
Express Mail Label No. EL538600728US

APPLICATION ELEMENTS *See MPEP chapter 600 concerning utility patent application contents.*	*ADDRESS TO:* **Assistant Commissioner for Patents Box Patent Application Washington, DC 20231**

1. ☒ Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)
2. ☒ Specification *Total Pages* 12
(preferred arrangement set forth below)
- Descriptive title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings *(if filed)*
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

3. ☒ Drawings *(35 USC 113) Total Sheets* 5
4. Oath or Declaration *Total Pages* 2
   a. ☒ Newly executed (original or copy)
   b. ☐ Copy from a prior application (37 CFR 1.63(d))
   (for continuation/divisional with Box 16 completed)
   i. ☐ DELETION OF INVENTOR(S)
   Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. ☐ Microfiche Computer Program *(Appendix)*
6. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. ☐ Computer Readable Copy
   b. ☐ Paper Copy (identical to computer copy)
   c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. ☒ Assignment Papers (cover sheet & document(s))
8. ☐ 37 CFR 3.73(b) Statement (when there is an assignee) ☐ Power of Attorney
9. ☐ English Translation Document (if applicable)
10. ☐ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS Citations
11. ☐ Preliminary Amendment
12. ☒ Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
13. ☐ Small Entity Statement(s) ☐ Statement filed in Prior Application, Status still proper and desired.
14. ☐ Certified Copy of Priority Document(s)
(if foreign priority is claimed)
15. ☐ Other

16. If a CONTINUING APPLICATION, *check appropriate box and supply the requisite information:*
☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No:
Prior Application Information: Examiner *Group / Art Unit:*
For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4B, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

17. CORRESPONDENCE ADDRESS

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Signature	J. Gustav Larson	Date	**November 28, 2000**

FEE TRANSMITTAL FOR FY 2001

Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT ($) 750.00

Complete if Known

Application Number	
Filing Date	
First Named Inventor	**Rosefield, et al.**
Group Art Unit	
Examiner Name	
Attorney Docket Number	**ATI010002**

METHOD OF PAYMENT (check one)

1. ☒ The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

Deposit Account Number	50-0441
Deposit Account Name	**ATI Technologies, Inc.**

☒ Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17

☒ Charge the Issue Fee Set in 37 CFR 1.18 at the mailing of the Notice of Allowance

☐ Applicant claims small entity status. See 37 CFR 1.27

2. ☐ Payment Enclosed:
☐ Check ☐ Money Order ☐ Other

FEE CALCULATION

1. FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	710	201	355	Utility filing fee	**710.00**
106	320	206	160	Design filing fee	
107	490	207	245	Plant filing fee	
108	710	208	355	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 710.00

2. CLAIMS

Claims	Extra	Fee from below	Fee Paid
Total **20**	(-20 =) **0**		
Indep. **3**	(- 3 =) **0**		
Multiple Dep.			

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	80	202	40	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim
109	80	209	40	Reissue independent claims over original patent
110	18	210	9	Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) .00

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	390	216	195	Extension for reply within second month	
117	890	217	445	Extension for reply within third month	
118	1,390	218	645	Extension for reply within fourth month	
128	1,890	228	945	Extension for reply within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	1550	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,240	241	620	Petition to revive - unintentional	
142	1,240	242	620	Utility issue fee (or reissue)	
143	440	243	220	Design issue fee	
144	600	244	300	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	40.00
146	710	246	355	Filing a submission after final rejection (37 CFR 1.129(a))	
149	710	249	355	For each additional invention to be examined (37 CFR 1.129(b))	
Other fee (specify)					
Other fee (specify)					

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 40.00

SUBMITTED BY: Simon, Fakhoury, Tangalos, Frantz & Galasso, PLC.				Complete (if applicable)	
Typed or Printed Name	**J. Gustav Larson, Reg. No. 39,8247**				
Signature	J. Gustav Larson	Date	**11-28-00**	Deposit Account User ID	

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Rosefield, et al. Examiner:

Serial No: Art Group:

Filing Date: Docket No: ATI010002

Title: APPARATUS HAVING REDUCED INPUT OUTPUT AREA AND METHOD THEREOF

To the Honorable Commissioner
of Patents and Trademarks
Washington, D.C. 20231

CERTIFICATE OF EXPRESS MAILING

Express Mail Label No. EL538600728US

Name of Depositor: **Terri Alloway**
(print or type)

Date of Deposit: November 28, 2000

Signature: Terri Alloway

I hereby certify that this paper and the items identified below are being deposited with the U.S. Postal Service "Express Mail Post Office to Addresses" service under 37 C.F.R. Section 1.10 on the 'Date of Deposit', indicated above, and is addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231.

Items accompanying this Certificate of Express Mailing:

☒ Filing papers for a new patent application, such filing papers include:

- ☒ A specification and drawings for a new patent application;
- ☒ Transmittal cover letter;
- ☒ Assignment agreement with Recordation Form Cover Sheet;
- ☒ Combined Declaration and Power of Attorney;
- ☐ Statement of Small Entity Status;
- ☐ Information Disclosure Statement;
- ☒ Return upon receipt post card;

PATENT APPLICATION
ATI010002

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

FILING OF A UNITED STATES PATENT APPLICATION

APPARATUS HAVING REDUCED INPUT OUTPUT AREA AND METHOD THEREOF

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Apparatus Having Reduced Input Output Area and Method Thereof

Field of the invention

The present invention relates generally to semiconductor devices, and more particularly to the layout of input output (IO) buffers associated with semiconductor devices.

Background of the Invention

Reduction in size of semiconductor devices continues to be an important objective in the design and manufacture of such devices. Generally, semiconductor devices comprise an input output (IO) ring and a logic core as illustrated in Figure 1. The logic core generally contains combinational and state machine logic to implement specific features of the semiconductor device. The IO ring generally contains signal buffers, and power buffers. Signal buffers include input buffers, output buffers, and bi-directional buffers. Input buffers receive and condition input signals from external to the semiconductor device for use by the logic core. Output buffers receive and condition output signals from the logic core for use external to the semiconductor device. Bi-directional buffers offer the functionality of both input buffers and output buffers. Power buffers provide fixed voltage references and/or supply voltages, such as Vdd and Vss to the semiconductor device.

The minimum number of power buffers needed by a semiconductor device is defined by the number of power buffers needed to prevent a supply voltage related failure from occurring for a specified maximum amount of direct current (DC) needed by the semiconductor device. Generally, supply voltage related failure mechanisms can occur. First, a power buffer can fail when it carries too much current. For example, a power buffer can be physically damaged when it carries too much current. Therefore, by increasing the number of power buffers used, the amount of current through each one can be reduced to assure the power buffers are not physically damaged. A second failure mechanism occurs when the inductance of bond wires prevents enough current from reaching the semiconductor device.

During high speed transitions in logic value, output buffer transistors can produce a high current. This high current, in turn, can impress a noise voltage on the low and high power supply buses as a result of a bonding wire, packaging and other inductances that prevent enough current from reaching the semiconductor device. Note that the impressed voltage is given by v=L (di/dt), where v is the noise voltage, L is the inductance of the bonding wire, packaging, etc., and di/dt is the derivative of the current generated by the large driver transistors of the output buffer with respect to time. Thus, the more rapidly that the current of large driver transistors vary in time, the greater the magnitude of the impressed noise signal. This undesirable noise voltage on the high and low power supply buses is commonly referred to as "ground bounce." A primary contributor to ground bounce is the bond wire connecting a die to its package. To limit the amount of ground bounce, the number of power buffers for the device are increased, which can result in a significant number of power buffers.

Prior art Figure 2 illustrates a semiconductor device having a logic core generally square in shape having seven IO devices on each side. Assuming that all the logic core area is used to implement features of the semiconductor device, the logic core device of Figure 2 is ideally laid out in that the combined width the 7 IO pads is equal to the width of the logic core. If the logic core illustrated in Figure 2 were smaller, and the same IO were needed, it would not be possible to reduce the overall size of the semiconductor device without changing the width of the IO buffers. The width of the IO buffers can be modified by relaying out each IO buffer. Relaying out buffers is not always a feasible option. Not only is relaying out IO buffers a time consuming process, but there is a practical limit to the extent that the width of IO buffers can be reduced.

Figure 3 illustrates three adjacent bond pads. The pitch between immediately adjacent bond pads of Figure 3 have a minimum distance, below which bonding to the pads cannot be properly performed. Therefore, the width of an IO buffer can be limited by the minimum pitch which must be maintained. In addition, Figure 3 illustrates that each IO buffer includes a bond pad area and an active buffer area, such that the bond pad areas form a bond pad ring within the IO ring illustrated in Figure 1.

Therefore, a method and/or apparatus capable of reducing the overall area utilized by the IO ring portion of a semiconductor device would be useful.

Brief Description of the Drawings

Figure 1 illustrates a floor plan of a semiconductor device in accordance with the prior art;

Figure 2 illustrates a more detailed embodiment of the prior art floor plan of Figure 1;

Figure 3 illustrates three IO buffers from the prior art IO ring of Figure 1;

Figure 4 illustrates a plan view of IO buffers in accordance with an embodiment of the present invention;

Figure 5 illustrates a plan view of IO buffers in accordance with another embodiment of the present invention; and

Figures 6 and 7 illustrate plan views of IO buffers in accordance with specific embodiments of the present invention.

It will be appreciated that for simplicity and clarity of illustration, elements illustrated in the drawings have not necessarily been drawn to scale. For example, the dimensions of some of the elements are exaggerated relative to other elements for clarity. Further, where considered appropriate, reference numerals have been repeated among the drawings to indicate corresponding or analogous elements.

Detailed Description of the Drawings

In accordance with a specific embodiment of the present invention, the number of bond pads for an IO ring of a semiconductor device is greater than the number of active

buffers associated with the bond pads. At least two of the bond pads are connected together so that the inductance at a pad connected to a reference or supply voltage is reduced. In other embodiments of the invention, the width of power buffers can vary from the width of input and output buffers. The present invention is described herein with specific embodiments illustrated in Figures 4-7.

Figure 4 illustrates a specific embodiment for a set of IO buffers 110 for reducing the overall area used by the IO ring. Specifically, Figure 4 illustrates five IO buffers 111-115. IO buffers 111-112, and 114-115 represent active buffers that receive and transmit signals to and from the logic core of the semiconductor device. IO buffer 113 is a power buffer used to provide a voltage reference to the semiconductor device. For example, buffer 113 will typically provide either a power or ground signal to the semiconductor device.

Each of the active buffers 111, 112, 114, and 115 have a common width (Wa), while the IO buffer 113 has a different width (Wp). The width of the active buffers 111, 112, 114, and 115 is generally based on the circuitry required within the active buffer portion 124. The logic portions within the active buffer portions 124 can include buffer-in logic, pre-driver logic, pre-buffer logic, output drivers, and input protection circuitry. Likewise, the width of the power buffer 113 is dictated by the circuitry used within its active area. However, since power buffers do not have to condition active signals, the circuitry required is generally limited to surge protection devices and interconnects. Therefore, the width of a power input output buffer can be less than the width of an active IO buffer.

Therefore, in the implementation illustrated in Figure 4, the overall area of an IO ring is reduced by allowing the power IO buffers to have a different width than the active IO buffers. In one implementation, the width of the power buffer will be limited by the minimum pad size needed for packaging. As illustrated, the pitch between the bond pad of power buffer 113 and the pitch between the bond pads of buffers 112 and 114 is a pitch P2, while the pitch between active buffers 111-112, and 114-115 is a larger pitch P1. Having a non-uniform pitch between bond pads requires packaging equipment capable of receiving specific locations for each bond pad, but allows for a reduction in the overall area of the IO ring.

Therefore, the specific implementation of Figure 4 makes it is possible to reduce the overall area occupied by the IO buffers through the use of power buffers having different widths and pitches than the other buffers.

Figure 5 illustrates a specific embodiment of a set of IO buffers 130 representing a portion of the overall area used by the IO ring. The buffer set 130 maintains a uniform pitch between the IO pads, thereby simplifying aspects of the packaging processes, and allowing a smaller overall pitch. However, variable widths are allowed within the active buffer area 144 of the buffers 131-133. Specifically, the width of the active buffer portion 144 of power buffer 132 is less than the width of the active buffer portion of buffers 131 and 133. This is possible because the area needed to implement the active buffer portion of a power buffer 132 is generally less than the area needed to implement an active buffer. In effect, there is an overlapping of the active buffer area 144 of active buffers 131 and 133 with the bond pad area 142 of power buffer 132. This overlap results in a smaller area utilized by the set of IO buffers 131-133, and thereby a smaller area utilized by the IO ring overall. Therefore, the implementation of IO buffers using the overlap methodology illustrated in Figure 5 allows for a common pitch to be maintained between the bond pads, and for the power buffer 132 to have a different active buffer area width. It will be appreciated that once laid out, the buffer set 130 can be treated as a single element during the layout of the IO ring. By allowing the width of the active area of power bond pads to vary from the width of active buffers it is possible to reduce the overall area of the IO ring.

Figure 6 illustrates a set of bonded IO buffers 150, such as may be part of a packaged device, representing a specific embodiment of reducing the overall area used by the IO ring of a semiconductor device. In accordance with the specific implementation of Figure 6, the number of bond pads for a given width of the IO ring is greater than the number of active buffer regions associated with the given width. In the specific implementation illustrated in Figure 6, five bond pads 171-175 are laid out in the same width as four active buffer areas 151-154.

As a result, in the embodiment illustrated, only four of the bond pads are directly connected to the active buffer regions 151-154 as illustrated by the shaded traces. The bond

pad 174 is not directly connected to an active buffer area, but is instead connected to the bond pad 172 by trace 189 within the bond pad ring portion 162 of the device to create an electrical connection. Note that in the embodiment illustrated, a portion of the trace is between the bond pads and the outer periphery of the die's IO ring. In another embodiment, the trace connecting the bond pads can be between the active region and the bond pads, or within the active region.

The primary influence on the number of power and ground buffers needed in a semiconductor device is the inductance of the bond wires from the package substrate to the semiconductor die. The effect of this inductance is to limit the amount of current that can be received over a specific period of time. In accordance with a specific embodiment of the present invention, a wire bond connection 182 is made between bond pad 172 and the package (not shown), and a wire bond connection 184 is made between bond pad 174 and the package substrate. In one embodiment, a portion of the package substrate provides a structure that allows for a power connection to be made. Such a structure may be a ring or individual structures that can be electrically connected, to which the wire bond connections 182 and 184 are connected. Because two wire bonds are used, the effective inductance seen by the power buffer 153 is effectively halved, resulting in a greater instantaneous current flow to the power buffer 153. Therefore, the use of two bond pads 172 and 174 as power bond pads has the effect of reducing the number of needed active power buffers by 1, since the single active power buffer will receive approximately twice the current. Therefore, in this implementation the size of the IO ring can be reduced by one power buffer.

An additional advantage of the layout of Figure 6 is that electrical cross talk between the signal received at pad 173 and signals received at pads 171 and 175 is reduced, since the distance between switching signals is increased, and a steady state on bond wires 182 and 184 can help isolate the signal on bond wire 183 from the other active signal. Note that in an alternate embodiment, more that one pad can reside between pads 172 and 174. For example, two or more pads can create a pad set that is immediately adjacent to the pads 172 and 174. Generally, each member of the pad set will be routed to its own active buffer.

Figure 7 illustrates another variation of the present invention, whereby the IO pads are staggered in two rows. For example, IO pads 191, 193, and 195 are in a first row, and IO pads 192 and 194 are in a second row. Staggering of IO pads allows an average effective pitch between the bond pads to be obtained that is less than the minimum pitch. For example, the distance between the pads in the first row can represent a minimum pad pitch. Likewise, the distance between the pads in the second row can represent a minimum pad pitch. However, because there are two rows, and the pads are offset from each other it is possible for the packaging equipment to properly bond each row of bond pads, and obtain the effective pitch (Pe) that is less than the minimum pitch. As illustrated in Figure 7, it is possible to connect two or more bond pads together using traces. For example, bond pads 192 and 194 are connected together. It will be appreciated that multiple bond pads and/or bond pads from different rows can be connected together. This allows for a reduced impedance to be seen by a single active buffer 183.

In the foregoing specification, the invention has been described with reference to specific embodiments. However, one of ordinary skill in the art appreciates that various modifications and changes can be made without departing from the scope of the present invention as set forth in the claims below. For example, the buffers and buffer sets described herein may be part of a standard library so that they may be reused and or modified easily. The package that the bond pads are connected to can be any one of a standard or proprietary package. Such a package may have power rings that the power pads connect to, or can have discrete power pads that the bond pads connect to. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of present invention.

Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential feature or element of any or all the claims

WHAT IS CLAIMED IS:

1. A method comprising the steps of:

receiving a minimum number of needed power bond pads;

determining a first number of power bond pads to be implemented, wherein the first number of power bond pads is greater than or equal to the minimum number; and

determining a second number of active buffer areas to be implemented for the power bond pads, wherein the second number is less than the first number.

2. The method of claim 1, further comprising the step of:

specifying a placement of a third number of immediately adjacent bond pads within a first distance along a periphery of a die, wherein the third number is less than the first number;

specifying a placement of a fourth number of immediately adjacent active buffer regions within the first distance along the periphery of the die, wherein the fourth number is less than the third number.

3. The method of claim 2, further comprising the step of:

specifying a placement of a trace connecting two bond pads of the immediately adjacent bond pads, wherein the two bond pads are not immediately adjacent to each other.

4. The method of claim 3, wherein the step of specifying the placement of the trace includes the placement of the trace being at least partially between the two bond pads and an outer periphery of a die.

5. A method comprising the steps of:

connecting a first bond pad to a first portion of a package, wherein the first portion of the package is to supply a predetermined voltage;

connecting a second bond pad to a second portion of a package, wherein the second portion of the package is to supply the predetermined voltage; and

wherein the first bond pad is connected to the second bond pad, and exactly one of the first bond pad and second bond pad is connected to an active buffer region, and a third bond pad is immediately adjacent to the second bond pad and to the first bond pad.

6. The method of claim 5, wherein the first portion of the package and the second portion of the package are electrically connected.

7. The method of claim 1, wherein a first pitch between the first bond pad and the third bond pad is less than an average pitch between buffers in the active buffer region.

8. The method of claim 1, wherein a first pitch between the first bond pad and the third bond pad is the same as a second pitch between the second bond pad and the third bond pad.

9. The method of claim 8, wherein the first pitch is a minimum allowable pitch.

10. The method of claim 8. wherein a fourth bond pad is immediately adjacent the second bond pad, and a third pitch between the second bond pad and the fourth bond pad is equal to the first pitch.

11. The method of claim 10, wherein the first pitch is a minimum allowable pitch.

12. The method of claim 8, wherein a fourth bond pad is immediately adjacent to the second bond pad, and a third pitch between the second bond pad and the fourth bond pad is different than the first pitch.

13. The method of claim 12, wherein the first pitch is a minimum allowable pitch.

14. An apparatus comprising:

semiconductor substrate having an input output (IO) ring, the IO ring having a bond pad portion and an active buffer portion;

the bond pad portion including:

a first bond pad;

a second set of bond pads having one or more bond pads;

a third bond pad, wherein the second set of bond pads is immediately adjacent to the first and third bond pads; and

a conductive trace coupling the first bond pad to the third bond pad.

15. The apparatus of claim 14, wherein the first bond pad and the third bond pad are power pads, wherein a power pad is to be coupled to a fixed voltage source.

16. The apparatus of claim 15, wherein the fixed voltage source is one of Vdd and Vss.

17. The apparatus of claim 14, further comprising:

a package substrate having a power portion, wherein the power portion is to provide a fixed voltage;

a first bond wire connected to the first bond pad and the power portion;

a second bond wire connected to the third bond pad and the power portion.

18. The apparatus of claim 17 further comprising exactly one of the first bond pad and the third bond pad being connected to the active buffer portion of the IO ring.

19. The apparatus of claim 14, wherein the second set of bond pads includes one bond pad.

20. The apparatus of claim 14, wherein the second set of bond pads includes more than one bond pads.

Abstract of the Disclosure

An input output ring for a semiconductor device is disclosed that uses power buffers having widths that vary from the widths of the input and output buffers. In one embodiment, the pitches between bond pads are the same, in another embodiment the pitches between the bond pads can vary. In another embodiment, the number of bond pads is greater than the number of associated active buffer areas. By connecting two power bond pads to a common buffer the inductance associated with the buffer is reduced, thereby reducing the number of active buffers needed to be dedicated to providing power to the semiconductor device.

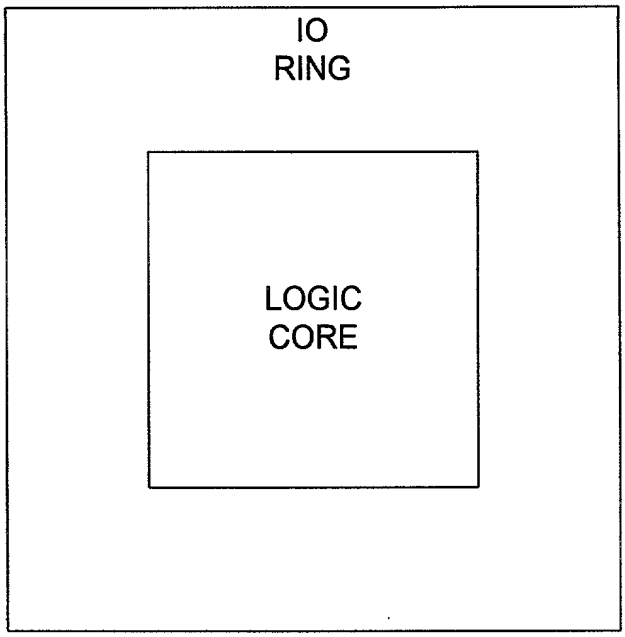

FIGURE 1

-- PRIOR ART --

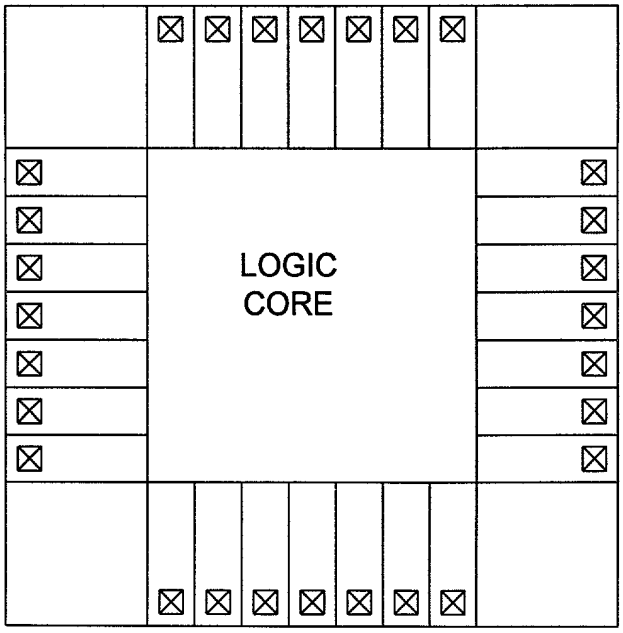

FIGURE 2

-- PRIOR ART --

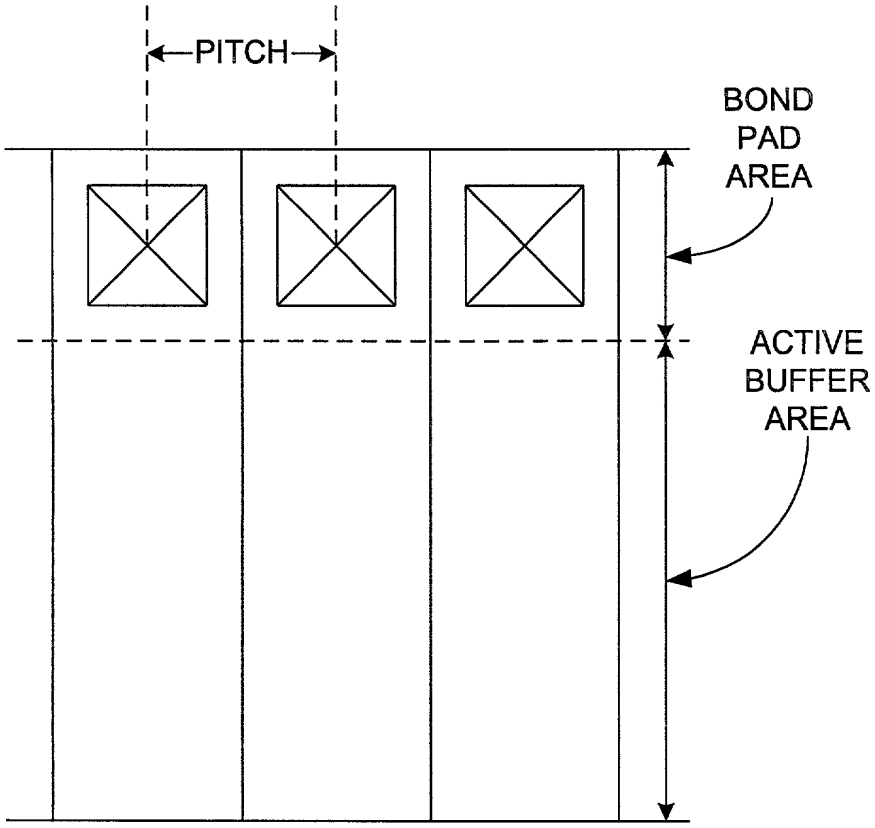

FIGURE 3

-- PRIOR ART --

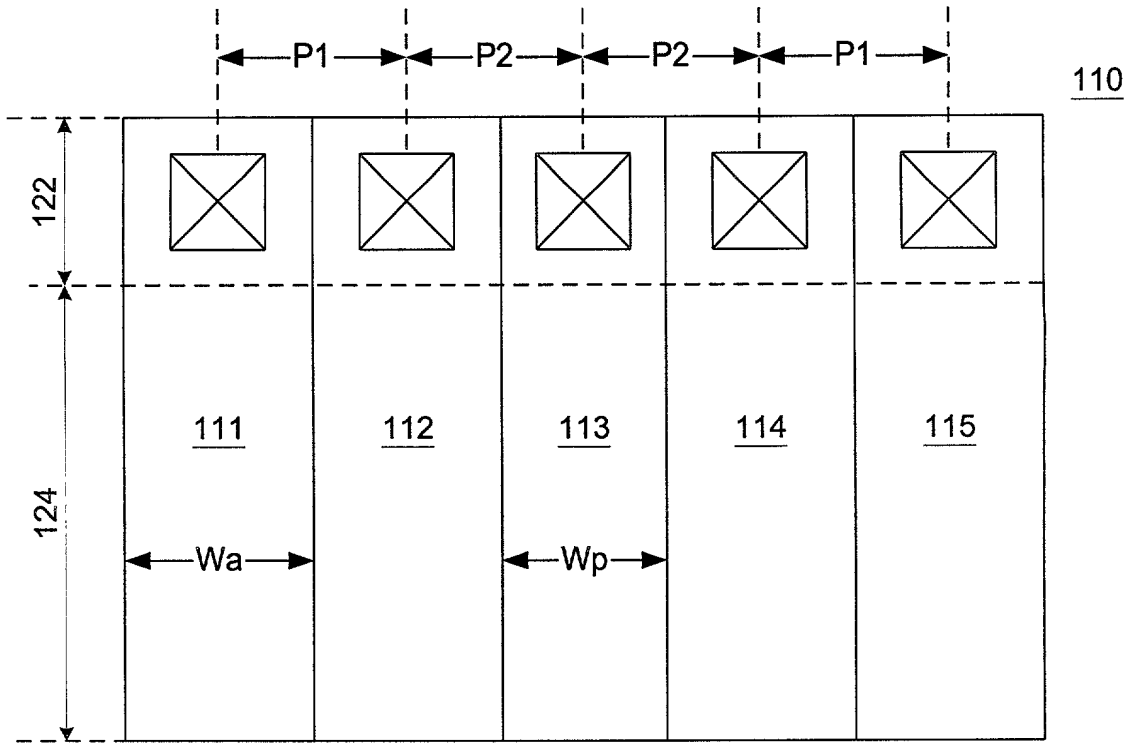

Figure 4

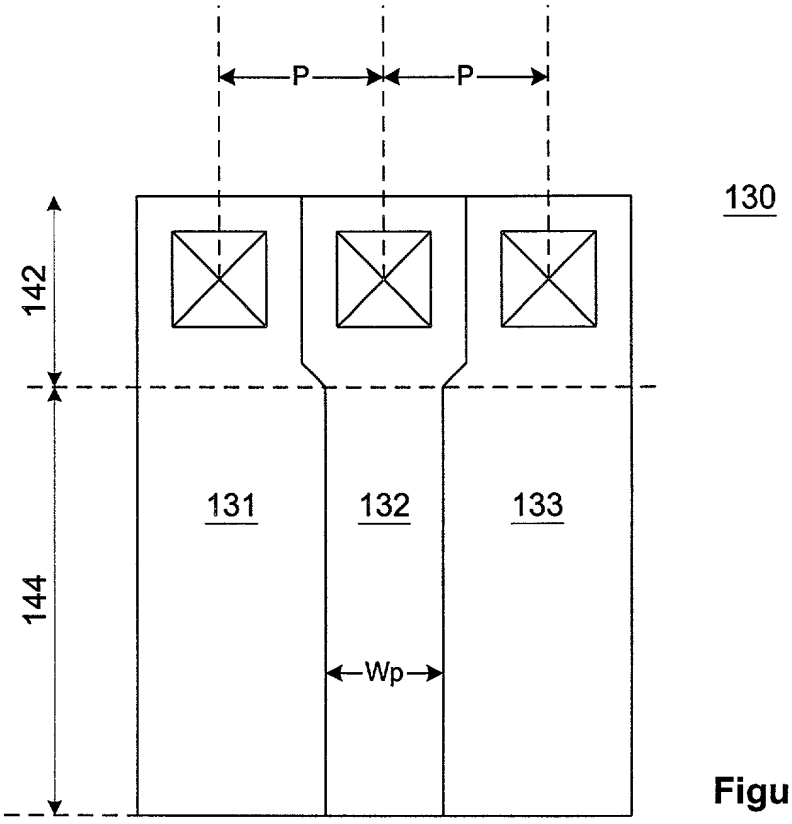

Figure 5

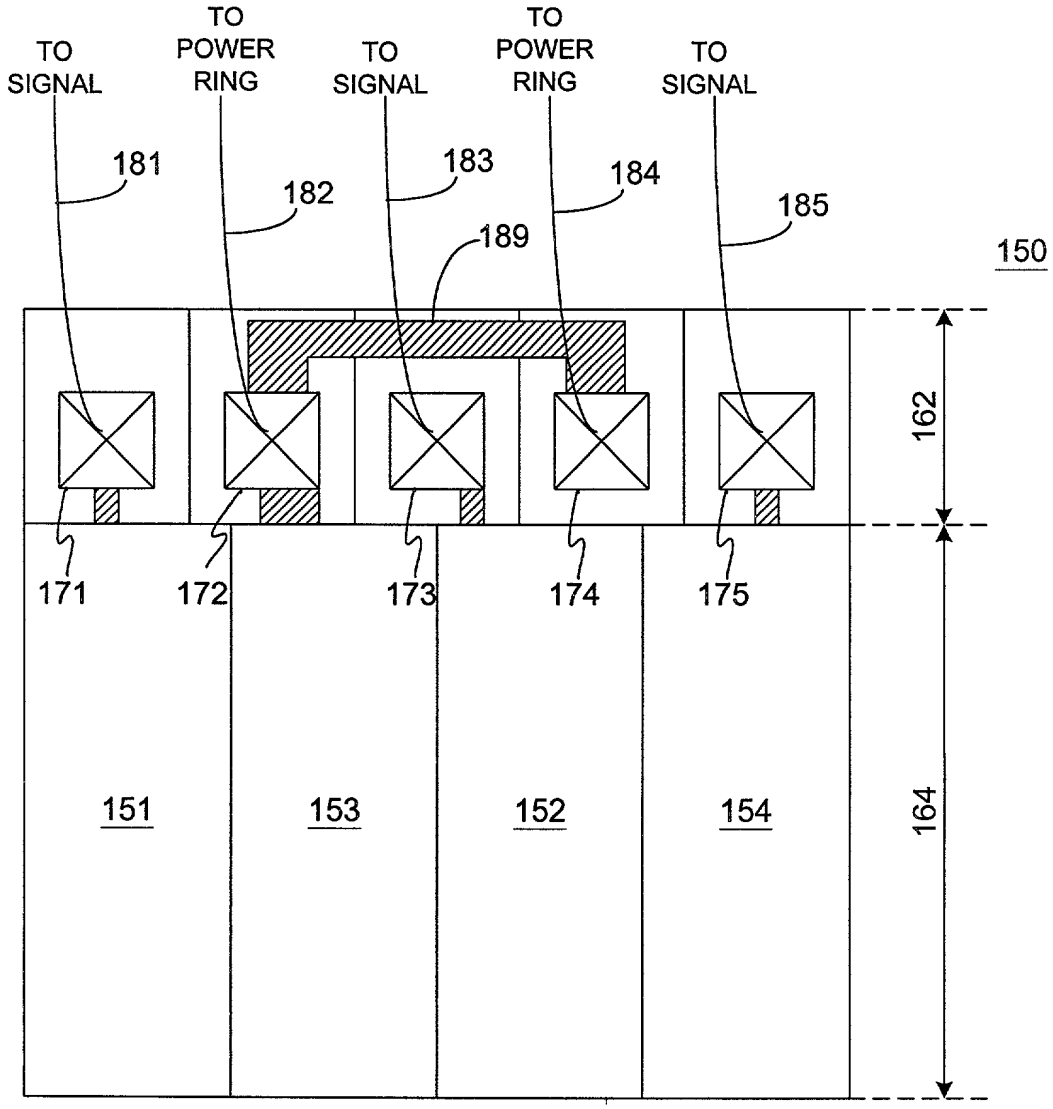
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Figure 6

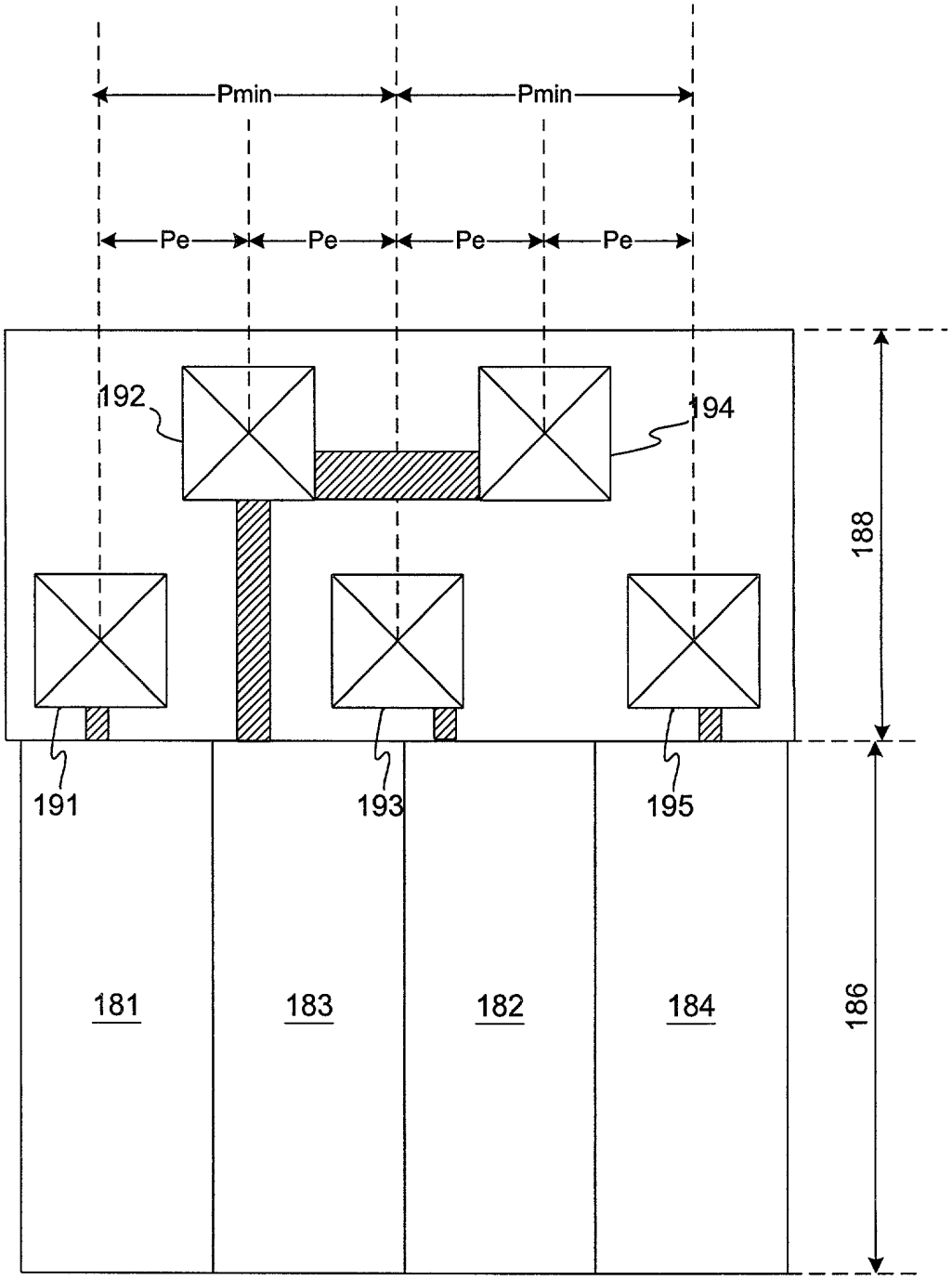

Figure 7

DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION
(37 CFR 1.63)

☒ Declaration Submitted with Initial Filing, OR
☐ **Declaration Submitted after Initial Filing**
(surcharge (37 CFR 1.16 (e)) required)

Attorney Docket Number ATI010002
First Named Inventor Rosefield, et al.
COMPLETE IF KNOWN
Application Number
Filing Date
Group Art Unit
Examiner Name

As a below named inventor, I hereby declare that:
My residence, post office address, and citizenship are as stated below next to my name.
I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

APPARATUS HAVING REDUCED INPUT OUTPUT AREA AND METHOD THEREOF

the specification of which:
☒ is attached hereto.
☐ was filed on (MM/DD/YYYY) as United States Application Number or PCT International Application Number and was amended on (MM/DD/YYYY) (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.
I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached? YES	NO
			☐	☐	☐
			☐	☐	☐

☐ Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

I hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application(s) listed below.

Application Number(s)	Filing Data (MM/DD/YYYY)

☐ Additional provisional application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

I hereby claim the benefit under 35 U.S.C. 120 of any United States application(s), or 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. Parent Application or PCT Parent Number	Parent Filing Date (MM/DD/YYYY)	Parent Patent Number (if applicable)

☐ Additional U.S. or PCT international application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

Attorney Docket No.: **ATI010002**

As a named inventor, I hereby appoint the following registered practitioner(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

Sally Daub, Reg. No. 41,478
J. Gustav Larson, Reg. No. 39,263

☐ Additional registered practitioner(s) named on supplemental Registered Practitioner Information sheet PTO/SB/02C attached hereto.

Direct all correspondence to:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Name of Sole or First Inventor: ☐ A petition has been filed for this unsigned inventor

Given Name (first and middle [if any])	Family Name or Surname
Peter L.	Rosefield

Inventor's Signature	Peter Rosefield		**Date**	21 Nov 2000
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Name of Additional Joint Inventor: ☐ A petition has been filed for this unsigned inventor

Given Name (first and middle [if any])	Family Name or Surname
Harvest W.C.	Chung

Inventor's Signature	Harvest Chung		**Date**	Nov 21/2000
Residence	City: Scarborough	State: Ontario	Country: Canada	Citizenship: Canadian
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City: Scarborough	State: Ontario	ZIP: M1H 3G6	Country: Canada	

☐ Additional inventors are being named on the _____supplemental Additional Inventor(s) sheet(s) PTO/SB/02A attached hereto.